CLAIMS:

What is claimed is:

1. A method of preventing processing errors due to invalid pointers, comprising:

fetching an instruction having a pointer operand for execution;

determining whether a trap flag corresponding to the pointer is in a set or reset condition; and

generating a trap control signal when the trap flag is in a reset condition.

2. The method according to claim 1, further comprising:

triggering a trap interrupt based on the trap control signal.

3. The method according to claim 1, further comprising:

executing the instruction.

4. The method according to claim 1, further comprising:

changing the trap flag corresponding to the pointer from the reset condition to the set condition based upon a write to the pointer.

5. The method according to claim 1, further comprising changing the trap flag to the reset condition after one of a power up of the processor or a reset of the processor.

6. A method of preventing processing errors due to invalid pointers, comprising:

providing trap flags, each corresponding to a pointer register;

resetting the trap flags upon one of a power up or reset; and

setting the trap flag corresponding to each pointer register based on the pointer register being written.

7. The method according to claim 6, further comprising:

generating a trap control signal when an instruction reads a pointer register with a trap flag set to reset.

8. The method according to claim 7, further comprising:

triggering a trap interrupt based on the trap control signal.

9. A processor that prevents processing errors due to invalid pointers, comprising:

instruction fetch and decode logic for fetching and decoding instructions;

registers;

trap flags, each corresponding to a register and each indicating a set or reset condition; and

a pointer trap coupled to the trap flags, the pointer trap generating a trap control signal based on decoding an instruction that reads a register that has a corresponding trap flag in a reset condition.

10. The processor according to claim 9, wherein the trap control signal is only generated when the register being read from is acting as a pointer register.

11. The processor according to claim 9, further comprising interrupt logic for generating an interrupt based on the trap control signal.

12. The processor according to claim 9, further comprising:

a reset/power up unit coupled to the trap flags, the reset/power on unit resetting the trap flags upon a reset/power up.

13. The processor according to claim 9, further comprising:

a trap flag control unit coupled to the trap flags, the trap flag control unit resetting the trap flags upon a reset/power up and setting each trap flag based on the corresponding register having been written by an instruction.